

**What is claimed is:**

1        1. A method for forming a trench isolation, comprising:  
2        providing a semiconductor substrate with a trench,  
3                wherein the semiconductor substrate has a mask  
4                layer;  
5        conformably forming a first insulating layer to cover  
6                the semiconductor substrate and the trench,  
7                wherein the trench is filled with the first  
8                insulating layer;  
9        anisotropically etching the first insulating layer to  
10               below the level of the semiconductor substrate;  
11        forming a second insulating layer to cover the  
12               semiconductor substrate and the trench; and  
13        planarizing the second insulating layer to expose the  
14               mask layer.

1        2. The method for forming a trench isolation as claimed  
2        in claim 1, wherein the mask layer is a nitride layer.

1        3. The method for forming a trench isolation as claimed  
2        in claim 1, wherein the first insulating layer is an oxide  
3        layer.

1        4. The method for forming a trench isolation as claimed  
2        in claim 3, wherein the first insulating layer is an LPCVD  
3        oxide layer.

1        5. The method for forming a trench isolation as claimed  
2        in claim 1, wherein the anisotropic etching is plasma etching  
3        or reactive ion etching.

1           6. The method for forming a trench isolation as claimed  
2     in claim 1, wherein the first insulating layer is lower than  
3     the semiconductor substrate by at least 300Å after anisotropic  
4     etching.

1           7. The method for forming a trench isolation as claimed  
2     in claim 1, wherein the second insulating layer is an oxide  
3     layer.

1           8. The method for forming a trench isolation as claimed  
2     in claim 7, wherein the oxide layer is a TEOS oxide layer.

1           9. The method for forming a trench isolation as claimed  
2     in claim 1, wherein the planarizing is chemical mechanical  
3     polishing.

1           10. A method for forming a trench isolation, comprising:  
2     providing a semiconductor substrate, wherein a pad  
3         layer, a mask layer, and a patterned photoresist  
4         layer with an opening are sequentially formed  
5         thereon;  
6     sequentially etching the mask layer, the pad layer, and  
7         the semiconductor substrate to form a trench using  
8         the patterned photoresist layer as a mask;  
9     removing the patterned photoresist layer;  
10    conformably forming an LPCVD oxide layer to cover the  
11         semiconductor substrate and the trench, wherein  
12         the trench is filled with the LPCVD oxide layer;  
13    anisotropically etching the LPCVD oxide layer to lower  
14         its surface below a top surface of the  
15    semiconductor substrate by at least 300Å;

16 forming an insulating layer to cover the semiconductor  
17 substrate and the trench, wherein the trench is  
18 filled with the insulating layer;  
19 planarizing the insulating layer to expose the mask  
20 layer; and  
21 removing the mask layer.

1 11. The method for forming a trench isolation as claimed  
2 in claim 10, wherein the pad layer is an oxide layer.

1 12. The method for forming a trench isolation as claimed  
2 in claim 10, wherein the mask layer is a nitride layer.

1 13. The method for forming a trench isolation as claimed  
2 in claim 10, wherein the aspect ratio of the trench is greater  
3 than 6.

1 14. The method for forming a trench isolation as claimed  
2 in claim 10, wherein the anisotropic etching is plasma etching  
3 or reactive ion etching.

1 15. The method for forming a trench isolation as claimed  
2 in claim 10, wherein the insulating layer is an oxide layer.

1 16. The method for forming a trench isolation as claimed  
2 in claim 15, wherein the oxide layer is a TEOS oxide layer.

1 17. The method for forming a trench isolation as claimed  
2 in claim 10, wherein the planarizing is a chemical mechanical  
3 polishing.

1 18. A method for forming a trench isolation, comprising:

2 providing a semiconductor substrate with a trench,  
3 wherein the semiconductor substrate has a mask  
4 layer;  
5 forming a first insulating layer to cover the  
6 semiconductor substrate and the trench;  
7 anisotropically etching the first insulating layer to  
8 form a spacer on a sidewall of the trench;  
9 forming a second insulating layer to cover the  
10 semiconductor substrate and the trench; and  
11 planarizing the second insulating layer to expose the  
12 mask layer.

1 19. The method for forming a trench isolation as claimed  
2 in claim 18, wherein the mask layer is a nitride layer.

1 20. The method for forming a trench isolation as claimed  
2 in claim 18, wherein the first insulating layer is an oxide  
3 layer.

1 21. The method for forming a trench isolation as claimed  
2 in claim 20, wherein the first insulating layer is an LPCVD  
3 oxide layer.

1 22. The method for forming a trench isolation as claimed  
2 in claim 18, wherein the anisotropic etching is plasma etching  
3 or reactive ion etching.

1 23. The method for forming a trench isolation as claimed  
2 in claim 18, wherein the spacer is lower than the semiconductor  
3 substrate.

1        24. The method for forming a trench isolation as claimed  
2        in claim 18, wherein the second insulating layer is an oxide  
3        layer.

1        25. The method for forming a trench isolation as claimed  
2        in claim 24, wherein the oxide layer is a TEOS oxide layer.

1        26. The method for forming a trench isolation as claimed  
2        in claim 18, wherein the planarizing is chemical mechanical  
3        polishing.

1        27. A method for forming a trench isolation, comprising:  
2        providing a semiconductor substrate, wherein a pad  
3        layer, a mask layer, and a patterned photoresist  
4        layer with an opening are sequentially formed  
5        thereon;  
6        sequentially etching the mask layer, the pad layer, and  
7        the semiconductor substrate to form a trench using  
8        the patterned photoresist layer as a mask;  
9        removing the patterned photoresist layer;  
10       conformably forming an LPCVD oxide layer to cover the  
11       semiconductor substrate and the trench;  
12       anisotropically etching the LPCVD oxide layer to form  
13       a spacer on a sidewall of the trench;  
14       forming an insulating layer to cover the semiconductor  
15       substrate and the trench;  
16       planarizing the insulating layer to expose the mask  
17       layer; and  
18       removing the mask layer.

1           28. The method for forming a trench isolation as claimed  
2           in claim 27, wherein the pad layer is an oxide layer.

1           29. The method for forming a trench isolation as claimed  
2           in claim 27, wherein the mask layer is a nitride layer.

1           30. The method for forming a trench isolation as claimed  
2           in claim 27, wherein the aspect ratio of the trench is greater  
3           than 6.

1           31. The method for forming a trench isolation as claimed  
2           in claim 27, wherein the anisotropic etching is plasma etching  
3           or reactive ion etching.

1           32. The method for forming a trench isolation as claimed  
2           in claim 27, wherein the spacer is lower than the semiconductor  
3           substrate.

1           33. The method for forming a trench isolation as claimed  
2           in claim 27, wherein the insulating layer is an oxide layer.

1           34. The method for forming a trench isolation as claimed  
2           in claim 33, wherein the insulating layer is a TEOS oxide layer.

1           35. The method for forming a trench isolation as claimed  
2           in claim 27, wherein the planarizing is performed by chemical  
3           mechanical polishing.

1           36. A method for forming a trench isolation, comprising:  
2           providing a semiconductor substrate, wherein a pad  
3           layer, a mask layer, and a patterned photoresist  
4           layer with a first opening and a second opening are  
5           sequentially formed thereon;

6 sequentially etching the mask layer, the pad layer, and  
7 the semiconductor substrate to form a first trench  
8 and a second trench using the patterned photoresist  
9 layer as a mask, wherein the aspect ratio of the  
10 first trench is greater than 6;  
11 removing the patterned photoresist layer;  
12 conformably forming an LPCVD oxide layer to cover the  
13 semiconductor substrate, the first trench, and the  
14 second trench, wherein the first trench is filled  
15 with the LPCVD oxide layer;  
16 anisotropical etching the LPCVD oxide layer to lower its  
17 surface below a top surface of the semiconductor  
18 substrate by at least 300Å;  
19 forming an insulating layer to cover the semiconductor  
20 substrate, the first trench and the second trench,  
21 wherein the first trench and the second trench are  
22 filled with the insulating layer;  
23 planarizing the insulating layer to expose the mask  
24 layer; and  
25 removing the mask layer.

1 37. The method for forming a trench isolation as claimed  
2 in claim 36, wherein the pad layer is an oxide layer.

1 38. The method for forming a trench isolation as claimed  
2 in claim 36, wherein the mask layer is a nitride layer.

1 39. The method for forming a trench isolation as claimed  
2 in claim 36, wherein the anisotropic etching is plasma etching  
3 or reactive ion etching.

1           40. The method for forming a trench isolation as claimed  
2 in claim 36, wherein the insulating layer is a TEOS oxide layer.

1           41. The method for forming a trench isolation as claimed  
2 in claim 36, wherein the planarizing is performed by chemical  
3 mechanical polishing.

1           42. A method for forming a trench isolation, comprising:  
2 providing a semiconductor substrate, wherein a pad  
3 layer, a mask layer, and a patterned photoresist  
4 layer with a first opening and a second opening are  
5 sequentially formed thereon;  
6 sequentially etching the mask layer, the pad layer, and  
7 the semiconductor substrate to form a first trench  
8 and a second trench using the patterned photoresist  
9 layer as a mask, wherein the aspect ratio of the  
10 first trench is greater than 6;  
11 removing the patterned photoresist layer;  
12 conformably forming an LPCVD oxide layer to cover the  
13 semiconductor substrate;  
14 anisotropically etching the LPCVD oxide layer to form  
15 a spacer on a sidewall of the first trench;  
16 forming an insulating layer to cover the semiconductor  
17 substrate, the first trench and the second trench;  
18 planarizing the insulating layer to expose the mask  
19 layer; and  
20 removing the mask layer.

1           43. The method for forming a trench isolation as claimed  
2 in claim 42, wherein the pad layer is an oxide layer.



1           44. The method for forming a trench isolation as claimed  
2 in claim 42, wherein the mask layer is a nitride layer.

1           45. The method for forming a trench isolation as claimed  
2 in claim 42, wherein the anisotropic etching is plasma etching  
3 or reactive ion etching.

1           46. The method for forming a trench isolation as claimed  
2 in claim 42, wherein the spacer is lower than the semiconductor  
3 substrate.

1           47. The method for forming a trench isolation as claimed  
2 in claim 42, wherein the insulating layer is a TEOS oxide layer.

1           48. The method for forming a trench isolation as claimed  
2 in claim 36, wherein the planarizing is chemical mechanical  
3 polishing.